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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): AUS920040058US1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on efiled on 01-16-2007

Signature /Louise Fay/

Typed or printed name Louise Fay

Application Number	Filed
10/809,594	03-25-2004

First Named Inventor: Lee

Art Unit	Examiner
2189	Shawn X. Gu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 48,504
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Theodore D. Fay III/
Signature

Theodore D. Fay III
Typed or printed name

972-385-8777
Telephone number

01-16-2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Lee**	§	Group Art Unit: **2189**
	§	
Serial No.: **10/809,594**	§	Examiner: **Shawn X. Gu**
	§	
Filed: **March 25, 2004**	§	Attorney Docket No.: **AUS920040058US1**
	§	

For: **Method to Allow PCI Host Bridge (PHB) to Handle Pre-Fetch Read Transactions on the PCI Bus Which Access System Memory Through Translation Control Entry (TCE) Table**

35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Respectfully submitted,

/Theodore D. Fay III/
Theodore D. Fay III
Registration No. 48,504

Duke W. Yee
Registration No. 34,285
YEE & ASSOCIATES, P.C.
P.O. Box 802333
Dallas, Texas 75380
(972) 385-8777
ATTORNEYS FOR APPLICANT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application: **Lee**	§	
	§	
Serial No.: **10/809,594**	§	Group Art Unit: **2189**
	§	
Filed: **March 25, 2004**	§	Examiner: **Shawn X. Gu**
	§	
For: **Method to Allow PCI Host Bridge (PHB) to Handle Pre-Fetch Read Transactions on the PCI Bus Which Access System Memory Through Translation Control Entry (TCE) Table**	§	Attorney Docket No.: **AUS920040058US1**
	§	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

35525
PATENT TRADEMARK OFFICE
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REASONS IN SUPPORT OF APPLICANTS' PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This document is submitted in support of the Pre-Appeal Brief Request for Review filed concurrently with a Notice of Appeal in compliance with 37 C.F.R. 41.31 and with the rules set out in the OG of July 12, 2005 for the New Appeal Brief Conference Pilot Program.

No fee or extension of time is believed due for this request. However, if any fee or extension of time for this request is required, Applicants request that this be considered a petition therefor. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund, to Deposit Account No. 09-0447.

REMARKS

Applicants hereby request a Pre-Appeal Brief Review (hereinafter "Request") of the claims finally rejected in the Final Office Action mailed October 13, 2006 as the rejections are clearly in error. The Request is provided herewith in accordance with the rules set out in the OG dated July 12, 2005.

I. Reasons Why the Rejections Are Clearly in Error

Dawkins et al., Method and Apparatus to Power Off and/or Reboot Logical Partitions in a Data Processing System, U.S. Patent Application Publication 2002/0124194 A1 (March 21, 2001) (hereinafter "*Dawkins*") fails to anticipate claim 1 because *Dawkins* does not teach each and every element recited in claim 1. Claim 1 is as follows:

> 1. A method in a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:
>
> reserving a page in system memory to form a reserved page;
>
> writing the reserved page;
>
> selecting a region in the system memory for the translation control entry table; and
>
> initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

Specifically, *Dawkins* does not teach "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page." The reasons why *Dawkins* does not teach these claimed features are presented in the previous response to office action. Applicants now rebut the examiner's arguments presented in the final office action of October 13, 2006 and thereby show that the rejection of claim 1 is clearly in error.

In response to the facts presented in the prior response to office action, the examiner states that:

> Regarding the Applicant's first argument (see Remarks, Pg.8, para.l), the Applicant states that "Dawkins does not teach 'writing the reserved page and initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page'". The Applicant

> further states that Dawkins does not teach these limitations because Dawkins does not verify that the reserved page is actually valid (see Remarks, Pg.9, para.1). However, verifying the entries is not a claimed feature of the invention, and the independent claims merely recite "... all entries are initialized to be valid ...". The Examiner interpreted the claims without considering the specific detail described in the specification (see specification, pg. 11) about how the entries are initialized to be valid and rejected the claims accordingly. To one ordinarily skilled the art, the TCE entries initialized by Dawkins' hypersivor [sic] to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid (see Dawkins, pg.4, para. [0046]. The Applicant must recite the features in the claims in order for them to be considered. The Applicant also argued that the initialization step is not inherently anticipated by Dawkins because this step is not necessarily present (see Remarks, pg.10, para. l), although the Examiner presented clear evidence that Dawkins explicitly, not inherently teaches this step as set forth in claims 1, 10 and 19's rejections. What is not necessarily present in the Applicant's admitted prior arts (see specification, pg.16, para.1) is clearly present in Dawkins' teaching.

Final Office Action of October 13, 2006, p. 7.

However, the examiner's response ignores the fact that *Dawkins* does not teach the claimed feature of initializing *all* entries in the TCE table, as required by claim 1. In fact, *Dawkins explicitly teaches otherwise*, as shown in the following portion of *Dawkins*, cited by the examiner as supposedly teaching this claimed feature:

> [0046] When platform 400 is initialized, a disjoint range of I/O bus DMA addresses is assigned to each of I/O adapters 448-462 for the exclusive use of the respective one of I/O adapters 448-462 by hypervisor 410. Hypervisor 410 then configures the terminal bridge range register (not shown) facility to enforce this exclusive use. Hypervisor 410 then communicates this allocation to the owning one of OS images 402-408. *Hypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a particular reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such*

> *that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408.*

Dawkins, paragraph 0046 (emphasis supplied) (citation to paragraph 0044 omitted as not relevant to the claim features at issue).

Dawkins teaches that the Hypervisor initializes all *entries in a particular I/O adapter's* ***associated section*** *of the TCE table to point to a particular reserved page per image that is owned by the OS image allocated to that I/O adapter. Dawkins* then teaches that by doing so *unauthorized access* to memory by an I/O adapter will not create an error that could affect one of the other OS images.

In stark contrast, claim 1 requires initializing ***all*** entries in the translation control table. Again, *Dawkins* only teaches initializing all entries ***in a particular I/O adapter's associated section*** of the translation control entry table. Because these two features are clearly different, the anticipation rejection is clearly in error. *Dawkins* does not anticipate claim 1 for this reason alone.

Additionally, *Dawkins* does not teach that all entries are *initialized to be valid*, as in claim 1. Instead, *Dawkins* teaches that the entries are initialized *to point to a particular reserved page per image.* Because these features are not equivalent, *Dawkins* does not anticipate claim 1.

Nevertheless, the examiner asserts that verifying the entries is not a claimed feature and that the examiner ignored the detail in the specification with regard to how the entries are initialized to be valid. However, the description of this claimed feature is not at issue, only the plain meaning of the claimed term. Claim 1 requires that the entries are initialized to be valid. *Dawkins* does not teach this claimed feature. The explicit disclosure is not present in *Dawkins*.

Nevertheless, the examiner states that, "To one ordinarily skilled the art, the TCE entries initialized by Dawkins' hypersivor [sic] to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid." Thus, the examiner appears to assert that *Dawkins* inherently teaches initializing all entries in the TCE to be valid, as in claim 1, because *Dawkins* teaches initializing TCE entries to prevent errors.

However, this interpretation of *Dawkins* is clearly in error. *Dawkins* specifically states that the entries are initialized, "such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images." Thus, *Dawkins* teaches that errors caused by *unauthorized access* are prevented – not that all errors are prevented and not that all entries are initialized to be valid, as in claim 1. Thus, again, *Dawkins* does not anticipate claim 1.

The remaining claims all contain features similar to those presented in claim 1. Therefore, the anticipation rejection of the remaining claims is also clearly in error.

Additionally, because *Dawkins* provides teachings that are explicitly different than the claimed features, *Dawkins* also does not suggest the claimed feature of, "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page." *Tanenbaum*, which is directed to operating systems, also does not teach or suggest these claimed features. The examiner does not assert otherwise. Therefore, the proposed combination of *Dawkins* and *Tanenbaum*, when considered as a whole, does not teach or suggest these claimed features. Accordingly, the obviousness rejections are also clearly in error.

II. Conclusion

For the reasons presented above, Applicants request that the rejections be withdrawn and the claims allowed. The Pre-Appeal Brief Conference Panel is invited to call the undersigned at the below-listed telephone number if in the opinion of the Panel such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 16, 2007

Respectfully submitted,

/Theodore D. Fay III/ TDF

Theodore D. Fay III
Reg. No. 48,504
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicant